REMARKS/DISCUSSION OF ISSUES

Claims 1-8 and 10-11 are pending in the application.

Reexamination and reconsideration are respectfully requested in view of the following remarks.

OBJECTION TO THE DRAWINGS

Applicant respectfully submits that the objection to the drawings is facially defective as it fails to assert even one supposed defect in the drawings that should be corrected.

The Office Action states that the drawings must show every feature of the invention specified in the claims.

However, the Office Action does not assert that the drawings in this application fail to show every feature of the invention. So, clearly, the Office Action also does not specify even one feature in any of the claims that is supposedly not shown in the Drawings.

Therefore, the Office Action fails to state any supposed defect in the drawings or any basis for objection thereto.

Accordingly, since the Office Action fails to state any basis for objecting to the claims or to identify anything in need or any correction, at this time Applicant considers the drawings not to have any objection thereto. If the Examiner has an actual basis for objection to the claims, he is invited to issue a new Office Action to put Applicant on notice of that basis of objection and the reasons therefore.

35 U.S.C. § 112, SECOND PARAGRAPH

The Office Action rejects claims 1-8 and 10 under 35 U.S.C. § 112, second paragraph.

Applicant respectfully traverses the rejections under 35 U.S.C. § 112, second paragraph, for at least the following reasons.

Applicant respectfully disagrees that the features of claim 1 are unclear, and

particularly disagrees that the "*optional aspect appears to read that the choice of ending the instruction or the reloading of the program counter is an optional step*."

No one of any skill in the art giving a fair reading of claim 1 – particularly in light of the knowledge available to one of skill in the art, and the teaching so the specification – would ever come to the tortured "reading" proposed in the Office Action – and for the very reason stated in the Office Action itself: "*The instruction must end or the system will hang and be useless*."

Clearly the Examiner already understands this, as indeed the Examiner correctly "interpreted" the claim when examining it – giving it the only possible meaningful interpretation, as anyone of skill in the art would do!. So Applicant respectfully cannot any basis for objection to a claim as being unclear when the Examiner himself fairly concedes that it has only one possible meaningful interpretation!

Accordingly, Applicant respectfully requests that the rejections of claims 1-8 and 10 under 35 U.S.C. § 112, second paragraph be withdrawn.

35 U.S.C. § 112, FIRST PARAGRAPH

The Office Action rejects claims 1-8 and 10 under 35 U.S.C. § 112, first paragraph.

Applicant respectfully traverses the rejections under 35 U.S.C. § 112, first paragraph, for at least the following reasons.

The Office Action states that there is no written description for the feature wherein the "*the program counter is reloaded with its current address or current value prior to ending the instruction*."

Applicant respectfully disagrees. Indeed, explicit support can be found, for example, at page 2, lines 27-29, page 3, line 1, and page 5, lines 3-5.

This alone satisfies the written description requirement of 35 U.S.C. § 112, first paragraph, and therefore renders the rejection improper.

However, for clarification, Applicant notes that the Examiner's statements at,

for example, page 5 lines 2-17 reflect a deep and profound misunderstanding of the claim and the disclosure. Applicant respectfully submits that the logic operation of reloading the at least one program counter with its current address or current value must indeed occur prior to ending the instruction. Otherwise, if, as stated by the Examiner, the previous (or present) instruction were executed again, it takes little thought to see that this would place the processor's operation into an infinite loop where the same instruction would be performed over and over and over again *ad infinitum*. However, this is not the case here. Rather, instead of just immediately ending an instruction in response to an unfulfilled branch condition, in the arrangement of claim 1, an optional step can be performed prior to ending the instruction wherein the current instruction is reloaded into the program counter. In either case – whether the instruction ends immediately or whether the program is reloaded first, the next operation is the execution of the subsequent instruction (not the same instruction all over again) in the program counter. This effectively does not alter the flow of the algorithm being executed, but it does alter the timing of the execution so that a branch operation and a don-not-branch operation consume more closely the same amount of time, thus making detection of cryptographic operations more difficult to analyze and attack. This is all explained in the specification.

Regarding claim 5, Applicant submits that the text cited above also provides support for the features of claim 5.

As to there being no discussion in the specification as to overwriting the program counter multiple times in one instruction, Applicant does not see where the claims recite overwriting the program counter multiple times in one instruction.

Accordingly, Applicant respectfully requests that the rejections of claims 1-8 and 10 under 35 U.S.C. § 112, first paragraph be withdrawn.

35 U.S.C. § 102 & 103

The Office Action rejects claims 1, 3-6, 8 and 10 under 35 U.S.C. § 102 over Cohen EP0690370 ("Cohen"), claims 2 and 11 under 35 U.S.C. § 103 over Cohen in

view of Delvaux et al. U.S. Patent 6,851,046 ("Delvaux"), and claim 7 under 35 U.S.C. § 103 over Cohen in view of Gammel DE 10044837 ("Gammel").

Applicant respectfully traverses these rejections for at least the following reasons.

Claim 1

Among other things, the microcontroller of claim 1 is adapted to execute a conditional branch instruction, wherein in case of a fulfilled branch condition at least one program counter is loaded with a new address or a new value, and in case of an unfulfilled branch condition the instruction is optionally either ended immediately, or the at least one program counter is reloaded with its current address or current value prior to ending the instruction.

Applicant respectfully submits that Cohen does not disclose any microprocessor including such a combination of features.

The Office Action cites page 8, line 41 – page 9, line 29, describing operation of the "jump unit" shown in FIG. 7 of Cohen.

However, the cited text does not describe any feature wherein in case of an unfulfilled branch condition the instruction is optionally either ended immediately, or the program counter is reloaded with its current address or current value prior to ending the instruction.

Indeed, there does not appear any option in Cohen's jump unit to end the instruction immediately: it always jumps to either a first location, a second location, and a third location (see Cohen at page 8, line 55 – page 9, line 4). The Office Action does not even appear to allege that it does, ignoring the plain language of claim 1. So Cohen cannot possibly disclose the microcontroller of claim 1!

The Office Action states that "*any instruction's execution, including that of a conditional branch, would result in a new address being loaded into the program counter if even to simply increment the program counter upon the completion of the current instruction*."

However, ***incrementing*** a counter upon completion of an instruction is not the same as ***loading*** the counter register with its current address or value prior to ending the instruction, as recited in claim 1. In general, during a program cycle of a microcontroller, a program counter's value is automatically incremented so that at the end of the instruction, the program counter automatically points to the next instruction to be performed. However, whenever a branch occurs, then a new address has to be loaded into the counter. This loading operation consumes a certain amount of time that is not required for automatic incrementation of the counter value. In the prior art, this causes a time difference for execution of the next instruction between: (a) a first case where no branch occurs and the address in the program counter is merely automatically incremented; and (b) a second case where a branch occurs and the branch address must be loaded into the program counter. Anyone of skill in the art who understands how a counter operates would clearly understand this principle.

In contrast, in the microcontroller of claim 1, optionally even when no branch occurs, the program counter is optionally reloaded with its current address prior to ending the instruction.

So, Applicant respectfully disagrees with the statement in the Office Action that any instruction's execution in Cohen would result in a new address being loaded into the program counter.

The Office Action also states that in the event that the condition is not fulfilled, then the jump instruction will jump to a location which could possibly be the current program counter address. However, this is not what is claimed, and – as explained above – if the same instruction was performed over again, then the processor would be trapped in an infinite loop.

Therefore, for at least these reasons, Applicant respectfully submits that Cohen does not disclose or suggest any microcontroller wherein in case of an unfulfilled branch condition the instruction is optionally either ended immediately, or the program counter is reloaded with its current address or current value prior to ending the instruction.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 1 is patentable over Cohen.

Claims 3-4

Claims 3-4 depend from claim 1 and are deemed patentable for at least the reasons set forth above with respect to claim 1. Applicant also specifically traverses the statement in the Office Action that a microcontroller is inherently a smartcard.

Claim 5

Among other things, the method of claim 1 includes comprising executing a conditional branch instruction, wherein in case of a fulfilled branch condition at least one program counter is loaded with a new address or a new value, and in case of an unfulfilled branch condition the instruction is optionally either ended immediately, or the at least one program counter is reloaded with its current address or current value prior to ending the instruction.

As explained above with respect to claim 1, Applicant respectfully submits that Cohen does not disclose such a combination of features.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 5 is patentable over Cohen.

Claims 6, 8 and 10

Claims 6, 8 and 10 depend from claim 5 and are deemed patentable for at least the reasons set forth above with respect to claim 5. Applicant also specifically traverses the statement in the Office Action that the recited special bit is inherently present in Cohen's robust jump instruction, for a variety of reasons, including the failure of Cohen to disclose that its apparatus of FIG. 7 supports both the robust jump instruction and a so-called "regular jump instruction" mentioned (without any citation) in the Office Action. Also, in any event the robust jump instruction pertains to a mechanism to verify the integrity of the instruction, and to ***jump to an address for an error routine*** when the integrity of the instruction has been compromised. This has nothing to do with determining whether to end an instruction immediately, or to reload a program counter with its current address or current value prior to ending the

instruction, which is controlled by the recited special bit.

Claim 2

Claim 2 depends from claim 1. Applicant respectfully submits that Delvaux does not remedy the shortcomings of Cohen as set forth above with respect to claim 1. Accordingly, claim 2 is deemed patentable for at least the reasons set forth above with respect to claim 1.

Claim 11

Among other things, the microcontroller of claim 11 includes a program counter and a multiplexer, wherein in case of a fulfilled branch condition the multiplexer is controlled to load the branch address into the program counter, and wherein in case of an unfulfilled branch condition the multiplexer is controlled to reload the program counter with its current address prior to ending the instruction.

No combination of the prior art remotely suggests that, in case of an unfulfilled branch condition, a multiplexer is controlled to reload the program counter with its current address prior to ending the instruction.

The Office Action cites Cohen page 8, line 41 – page 9, line 29 as supposedly disclosing this feature. Of course, this is impossible since Cohen does not even disclose any multiplexer – as the Office Action fairly admits.

The Office Action also cites FIG. 1D of Delvaux as supposedly showing this feature. FIG. 1D of Delvaux does show a MUX 116, but it does not show any multiplexer that, wherein in case of an unfulfilled branch condition, is controlled to reload the program counter with its current address prior to ending the instruction. In particular, it is plainly shown that MUX 116 is controlled to increment the program counter by adding "1" to the previous program count value with adder 112.

Accordingly, Applicant respectfully submits that claim 11 is clearly patentable over the cited prior art.

Claim 7

Claim 7 depends from claim 5. Applicant respectfully submits that Gammel does not remedy the shortcomings of Cohen as set forth above with respect to claim 5. Accordingly, claim 7 is deemed patentable for at least the reasons set forth above with respect to claim 5.

Furthermore, the Office Action cites nothing in either Cohen or Gammel; that discloses the ***actual*** features recited in claim 7, namely, at least one of testing of the branch condition or the loading of the program counter is carried out with complementary data. In particular, merely transmitting a bit between a first and a second circuit block is not the same as testing a branch condition or loading a program counter.

Applicant also traverse the proposed combination of Cohen and Gammel as apparently being based on nothing but hindsight reconstruction of Applicant's invention using Applicant's own teachings, as the Office Action is devoid of any evidence that the supposed reason for the proposed combination would have been apparent to anyone of ordinary skill in the art at the time of Applicant's invention.

Accordingly, for at least these additional reasons, Applicant respectfully submits that claim 7 is patentable over the cited art.

CONCLUSION

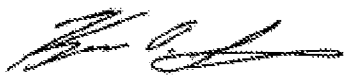
In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1-8 and 10-11 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this reply to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17,

particularly extension of time fees.

Respectfully submitted,

VOLENTINE & WHITT



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